

**GigaDevice Semiconductor Inc.**

**GD30LD1031x**  
**3A, 6.5V, Low Input Voltage, LDO**

Datasheet

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## 1 Features

- Input Voltage Range, 1.4 V to 6.5 V
- Output Voltage Range, 0.5 V to 5.2 V, Set by a Resistor Divider
- Accurate Output Voltage Accuracy: 1%, Over Line, Load and Temperature
- Ultra Low Dropout Voltage: Maximum 300 mV at 3A
- Current Limit Function
- Short Circuit Protection
- Enable Function

## 2 Applications

- Wireless Infrastructure
- Telecom/Networking Cards
- Industrial Application
- Set Top Box
- Medical Equipment
- Notebook Computers
- Battery Powered Systems

## 3 General description

The GD30LD1031x is a high-current, high accuracy, low-dropout linear regulator (LDO) capable of sourcing 3A with extreme low dropout (max, 300mV).

The device output voltage is adjustable from 0.5 V to 5.2 V using the external resistor divider. The device supports input supply voltage as low to 1.4 V. Additionally, the GD30LD1031x has an enable pin to further reduce power dissipation while shutdown.

The GD30LD1031x provides excellent regulation over variations in line, load and temperature. The output voltage can be set by an external divider depending on how the FB pin is configured.

The device is fully specified over the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and is offered in the TO263(Exposed Pad) package.

## 4 Device overview

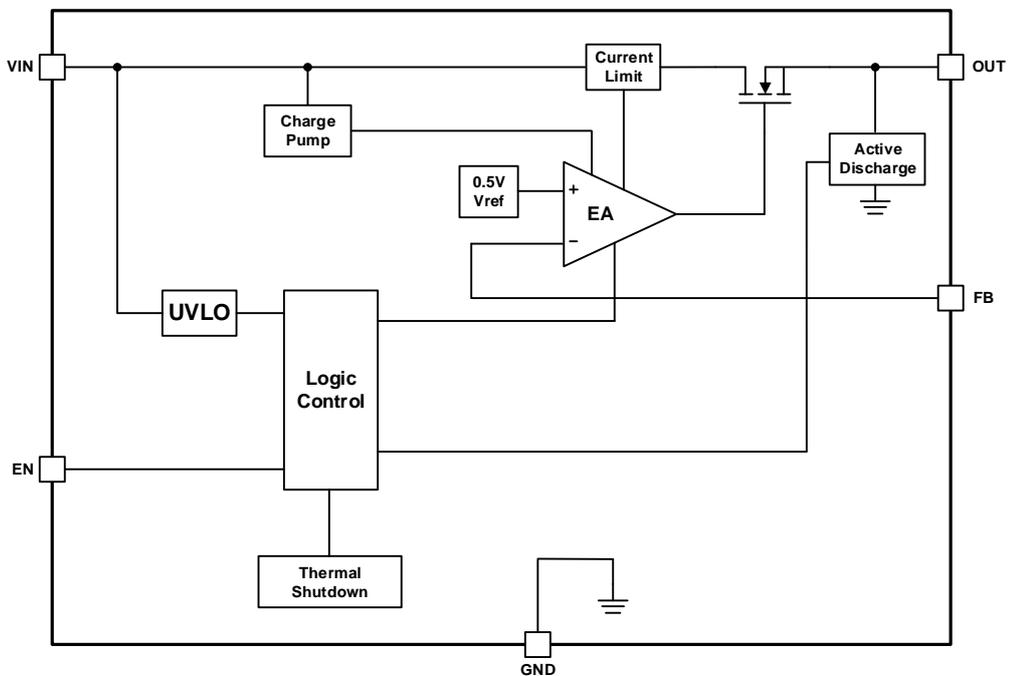
### 4.1 Device information

Table 4-1 Device information for GD30LD1031x

| Part Number | Package | Function            | Description                                     |
|-------------|---------|---------------------|---|
| GD30LD1031x | TO263   | With enable pin(EN) | 3A Low input voltage, low dropout LDO regulator |

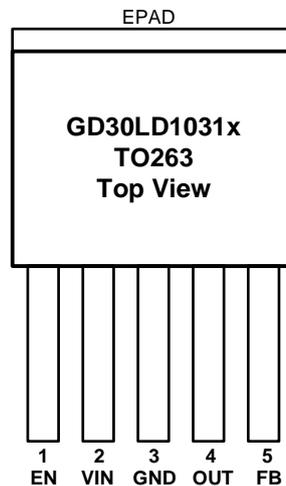
### 4.2 Block diagram

Figure 4-1 Block diagram for GD30LD1031x



### 4.3 Pinout and pin assignment

Figure 4-2 GD30LD1031x TO263 pinouts



### 4.4 Pin definitions

Table 4-2 GD30LD1031x TO263 pin definitions

| Pin Name | Pins    | Pin Type | Functions description   |
|----------|---------|----------|---|
| EN       | 1       | I        | <b>Enable Control Input.</b> Connecting this pin to logic high enables the regulator, and driving this pin low puts it into shutdown mode.  |
| VIN      | 2       | I        | <b>Supply Input.</b> A general 10uF or larger ceramic capacitor should be placed as close as possible to this pin for better noise rejection.   |
| GND      | 3       | G        | <b>Ground.</b> The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.  |
| OUT      | 4       | O        | <b>Output of the Regulator.</b> The larger ceramic capacitor (47uF or greater) is stable. Place the output capacitor as close to the device as possible. Minimize the impedance between V <sub>OUT</sub> pin to load. |
| FB       | 5       | O        | <b>Feedback Voltage Input.</b> This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.5V typically.  |
| GND      | 6(EPAD) | G        | Device power ground.  |

**Notes:**

1. Type: I = input, O = output, G = Ground.

## 5 Functional description

### 5.1 Output Voltage Setting

The output voltage of the GD30LD1031x can be set by external resistors to achieve different output targets.

By using external resistors, the output voltage is determined by the values of R1 and R2 as shown in [Figure 7-1](#). The values of R1 and R2 can be calculated for any voltage value using the following formula:

$$V_{\text{OUT}} = V_{\text{FB}} \times \left( 1 + \frac{R_1}{R_2} \right)$$

### 5.2 Chip Enable Operation

The GD30LD1031x goes into sleep mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and band gap are all turned off, reducing the supply current to only 25uA(max). The EN pin can be directly tied to keep the part on.

### 5.3 Recommended device selection

#### 5.3.1 C<sub>IN</sub> and C<sub>OUT</sub> Selection

The GD30LD1031x is designed to support low-series resistance (ESR) ceramic capacitors. It is recommended to use ceramic capacitors with X7R, X5R, and C0G-rated ceramic capacitors to get good capacitive stability across different temperatures.

However, the capacitance of ceramic capacitors varies with operating voltage and temperature, and the design engineer must be aware of these characteristics. Ceramic capacitors are usually recommended to be derated by 50%. A 47μF or greater output ceramic capacitor is suggested to ensure stability. Input capacitance is selected to minimize transient input drop during load current steps. For general applications, an input capacitor of at least 10μF is highly recommended for minimal input impedance. If the trace inductance between the GD30LD1031x input pin and power supply is high, a fast load transient can cause V<sub>IN</sub> voltage level ringing above the absolute maximum voltage rating which damages the device. Adding more input capacitors is available to restrict the ringing and keep it below the device absolute maximum ratings.

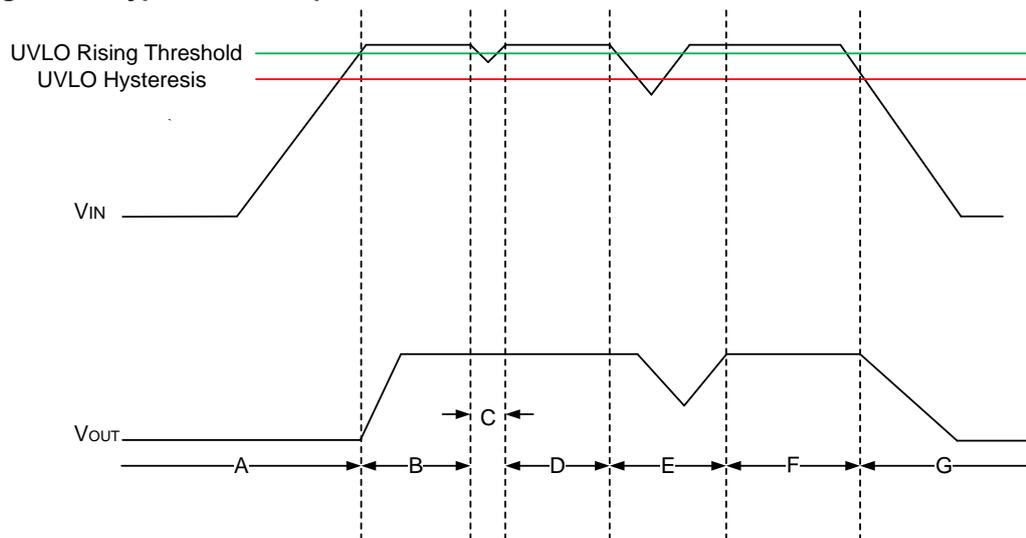
Generally, a 47μF 0805-sized ceramic capacitor in parallel with two 10μF 0805-sized ceramic capacitor ensures the minimum effective capacitance at high input voltage and high output voltage requirement. Place these capacitors as close to the pins as possible for

optimum performance and to ensure stability.

## 5.4 Undervoltage Lockout (UVLO)

The UVLO circuits ensure that the device stays disabled before its input reach the minimum operational voltage range, and ensures that the device properly shuts down when either the input collapses. Figure 5-1 and Table 5-1 explain one of the UVLO circuits being triggered to various input voltage events, assuming  $V_{EN} \geq V_{IH(EN)}$ .

**Figure 5-1 Typical UVLO Operation**



**Table 5-1 Typical UVLO Operation Description**

| Region | EVENT  | VOUT STATUS | COMMENT   |
|--------|--|-------------|---|
| A      | Turn on,<br>$V_{IN} \geq V_{UVLO\_1,2(IN)}$ and                  | Off         | Startup   |
| B      | Regulation   | On          | Regulates to target $V_{OUT}$   |
| C      | Brown out,<br>$V_{IN} \geq V_{UVLO\_1,2(IN)} - V_{HYS\_1,2(IN)}$ | On          | The output can fall out of regulation but the device is still enabled   |
| D      | Regulation   | On          | Regulates to target $V_{OUT}$   |
| E      | Brown out<br>$V_{IN} < V_{UVLO(IN)} - V_{HYS(IN)}$               | Off         | The device is disabled and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO fault is removed when either the IN rising threshold is reached by the input a normal start-up then follows |
| F      | Regulation   | On          | Regulates to target $V_{OUT}$   |

|   |  |     |  |
|---|--|-----|--|
| G | Turn off,<br>$V_{IN} < V_{UVLO(IN)} - V_{HYS(IN)}$ | Off | The output falls because of the load and active discharge circuit. |
|---|--|-----|--|

Similar to many other LDOs with this feature, the UVLO circuits take a few microseconds to fully assert. During this time, a downward line transient below approximately 0.8V causes the UVLO to assert for a short time; however, the UVLO circuits do not have enough stored energy to fully discharge the internal circuits inside of the device. When the UVLO circuits are not given enough time to fully discharge the internal nodes, the outputs are not fully disabled.

The effect of the downward line transient can be mitigated by using a larger input capacitor to increase the fall time of the input supply when operating near the minimum  $V_{IN}$ .

## 5.5 Power Dissipation ( $P_D$ )

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

$V_{IN} \times I_{GND}$  represents the static power consumption of the LDO, the value is relatively small and can be ignored. An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ( $T_J$ ) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $\theta_{JA}$ ) of the combined PCB, device package, and the temperature of the ambient air ( $T_A$ ).

$$T_J = T_A + \theta_{JA} \times P_D$$

$$I_{OUT} = (T_J - T_A) / [\theta_{JA} \times (V_{IN} - V_{OUT})]$$

## 6 Electrical characteristics

### 6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6-1 Absolute maximum ratings**

| Symbol                  | Parameter           | Min                | Max | Unit |
|-------------------------|---------------------|--------------------|-----|------|
| Voltage                 | IN, EN, OUT         | -0.3               | 7.0 | V    |
|                         | FB                  | -0.3               | 3.6 | V    |
| Current                 | OUT                 | Internally limited |     | A    |
| Thermal characteristics |                     |                    |     |      |
| T <sub>stg</sub>        | Storage temperature | -65                | 150 | °C   |

### 6.2 Recommended Operating Conditions

**Table 6-2 Recommended Operating Conditions**

| Symbol           | Parameter                      | Min | Typ | Max | Unit |
|------------------|--------------------------------|-----|-----|-----|------|
| V <sub>IN</sub>  | Input voltage range            | 1.4 | —   | 6.5 | V    |
| V <sub>OUT</sub> | Output voltage range           | 0.5 | —   | 5.2 | V    |
| V <sub>EN</sub>  | Enable Voltage range           | 0   | —   | 6.5 | V    |
| I <sub>OUT</sub> | Output current                 | 0   | —   | 3   | A    |
| C <sub>IN</sub>  | Input capacitor                | —   | 10  | —   | uF   |
| C <sub>OUT</sub> | Output capacitor               | —   | 47  | —   | uF   |
| T <sub>J</sub>   | Operating junction temperature | -40 | —   | 125 | °C   |

## 6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample.

**Table 6-3 Electrostatic Discharge characteristics**

| Symbol         | Parameter   | Conditions  | Value      | Unit |
|----------------|---|---|------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model)    | $T_A = 25\text{ }^\circ\text{C}$ ;<br>JS-001-2017 | $\pm 2000$ | V    |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A = 25\text{ }^\circ\text{C}$ ;<br>JS-002-2018 | $\pm 500$  | V    |

## 6.4 Electrical Specifications

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ), Typical values are at  $T_J = 25^\circ\text{C}$ .  $V_{IN} = 1.4\text{ V}$  or  $V_{IN} = V_{OUT(TARGET)} + 0.4\text{ V}$ ,  $V_{OUT(TARGET)} = 0.5\text{ V}$ ,  $V_{OUT}$  connected to  $50\ \Omega$  to GND,  $V_{EN} = 1.4\text{ V}$ ,  $C_{IN} = 10\ \mu\text{F}$ ,  $C_{OUT} = 47\ \mu\text{F}$ , unless otherwise noted.

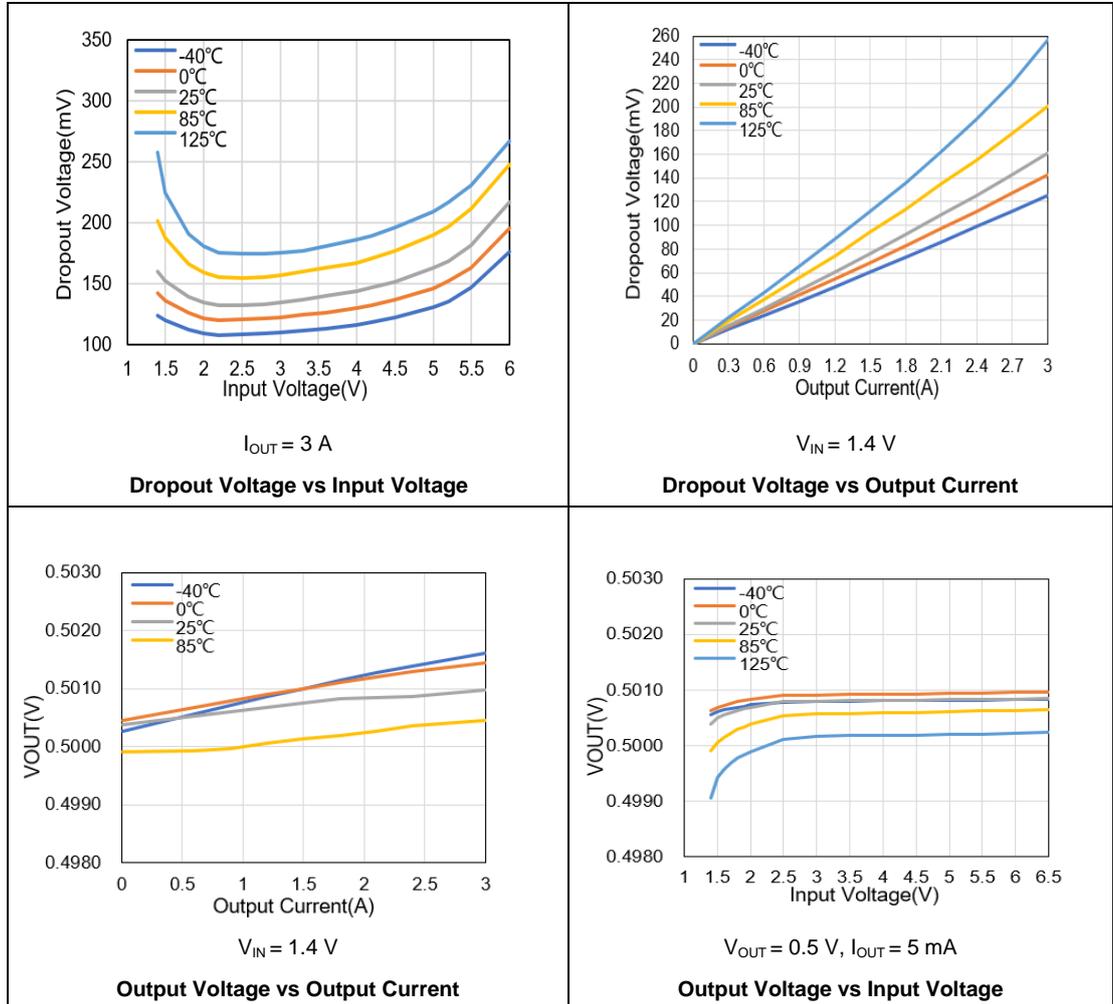
**Table 6-4 Electrical characteristics**

| Symbol                                  | Parameter            | Conditions   | Min        | Typ  | Max        | Unit |
|---|----------------------|--|------------|------|------------|------|
| $V_{IN}$                                | Input Range          | —  | 1.4        | —    | 6.5        | V    |
| $V_{FB}$                                | Feedback Voltage     | —  | —          | 0.5  | —          | V    |
| $V_{UVLO(IN)}$                          | UVLO                 | $V_{IN}$ rising  | —          | 1.33 | 1.39       | V    |
| $V_{HYS(IN)}$                           | UVLO hysteresis      | —  | —          | 230  | —          | mV   |
| $V_{OUT}$                               | Output Voltage Range | Using external resistors   | 0.5<br>-1% | —    | 5.2<br>+1% | V    |
|   | Output Accuracy      | $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,<br>$0.5\text{ V} \leq V_{OUT} \leq 5.2\text{ V}$ | -1         | —    | 1          | %    |
| $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$  | Line Regulation      | $I_{OUT} = 5\text{ mA}$ ,<br>$1.4\text{ V} \leq V_{IN} \leq 6.5\text{ V}$            | —          | 0.1  | —          | mV/V |
| $\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$ | Load Regulation      | $5\text{ mA} \leq I_{OUT} \leq 3\text{ A}$   | —          | 0.3  | —          | mV/A |
| $V_{DROPO}$                             | Dropout Voltage      | $V_{IN} = 1.4\text{ V}$ , $I_{OUT} = 3\text{ A}$ ,<br>$V_{FB} = 0.5\text{ V} - 3\%$  | —          | 120  | 250        | mV   |
|   |                      | $V_{IN} = 5.6\text{ V}$ , $I_{OUT} = 3\text{ A}$ ,<br>$V_{FB} = 0.5\text{ V} - 3\%$  | —          | 150  | 300        | mV   |
| $I_{LIM}$                               | Output Current Limit | $V_{OUT} = 90\% * V_{OUT(TARGET)}$<br>$V_{IN} = V_{OUT(TARGET)} + 400\text{ mV}$     | —          | 4.2  | —          | A    |

| Symbol                      | Parameter                  | Conditions                                   | Min  | Typ | Max | Unit        |
|-----------------------------|----------------------------|--|------|-----|-----|-------------|
| Short-Circuit Current Limit | $I_{SC}$                   | $R_{LOAD} = 20m\Omega$                       | —    | 1.0 | —   | A           |
| $I_{GND}$                   | Ground Pin Current         | $V_{IN} = 6.5 V, I_{OUT} = 5 mA$             | —    | 3.0 | 4.2 | mA          |
|                             |                            | $V_{IN} = 1.4 V, I_{OUT} = 3A$               | —    | 4.2 | 5.5 | mA          |
|                             |                            | Shutdown<br>$V_{IN} = 6.5 V, V_{EN} = 0.5 V$ | —    | —   | 25  | $\mu A$     |
| $I_{EN}$                    | EN Pin Current             | $V_{IN} = 6.5 V, V_{EN} = 0 V$<br>and 6.5 V  | -0.1 | —   | 0.1 | $\mu A$     |
| $V_{EN\_H}$                 | EN Pin High-Level          | —  | 1.1  | —   | 6.5 | V           |
| $V_{EN\_L}$                 | EN Pin Low-Level           | —  | 0    | —   | 0.5 | V           |
| $I_{FB}$                    | FB Pin leakage Current     | $V_{IN} = 6.5 V$                             | -100 | —   | 100 | nA          |
| $T_{SD}$                    | Thermal Shutdown Threshold | Shut down, temperature increasing            | —    | 160 | —   | $^{\circ}C$ |
|                             |                            | Reset, temperature increasing                | —    | 140 | —   | $^{\circ}C$ |

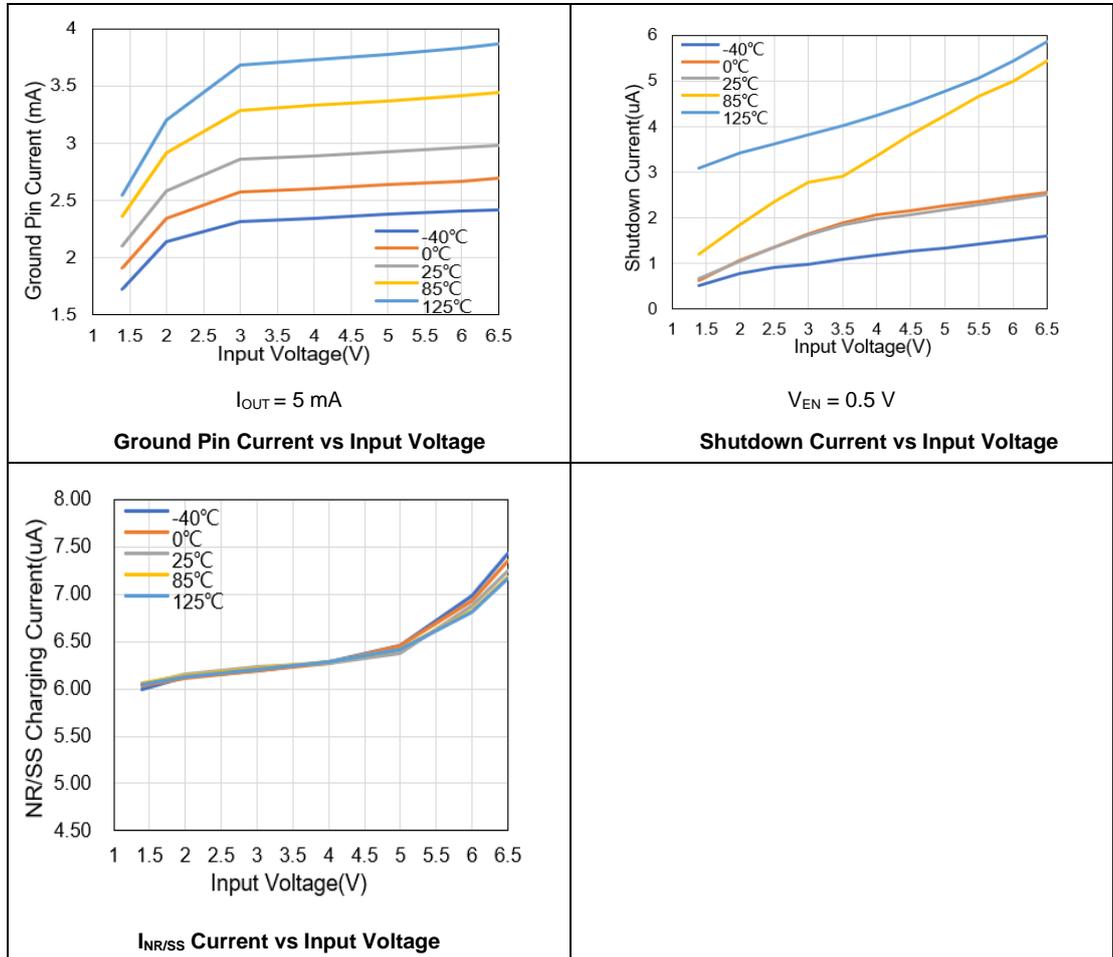
## 6.5 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 1.4\text{ V}$  or  $V_{IN} = V_{OUT(NOM)} + 0.4\text{ V}$  (whichever is greater),  $V_{OUT(NOM)} = 0.5\text{ V}$ ,  $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 47\text{ }\mu\text{F} // 10\text{ }\mu\text{F} // 10\text{ }\mu\text{F}$  (unless otherwise noted).



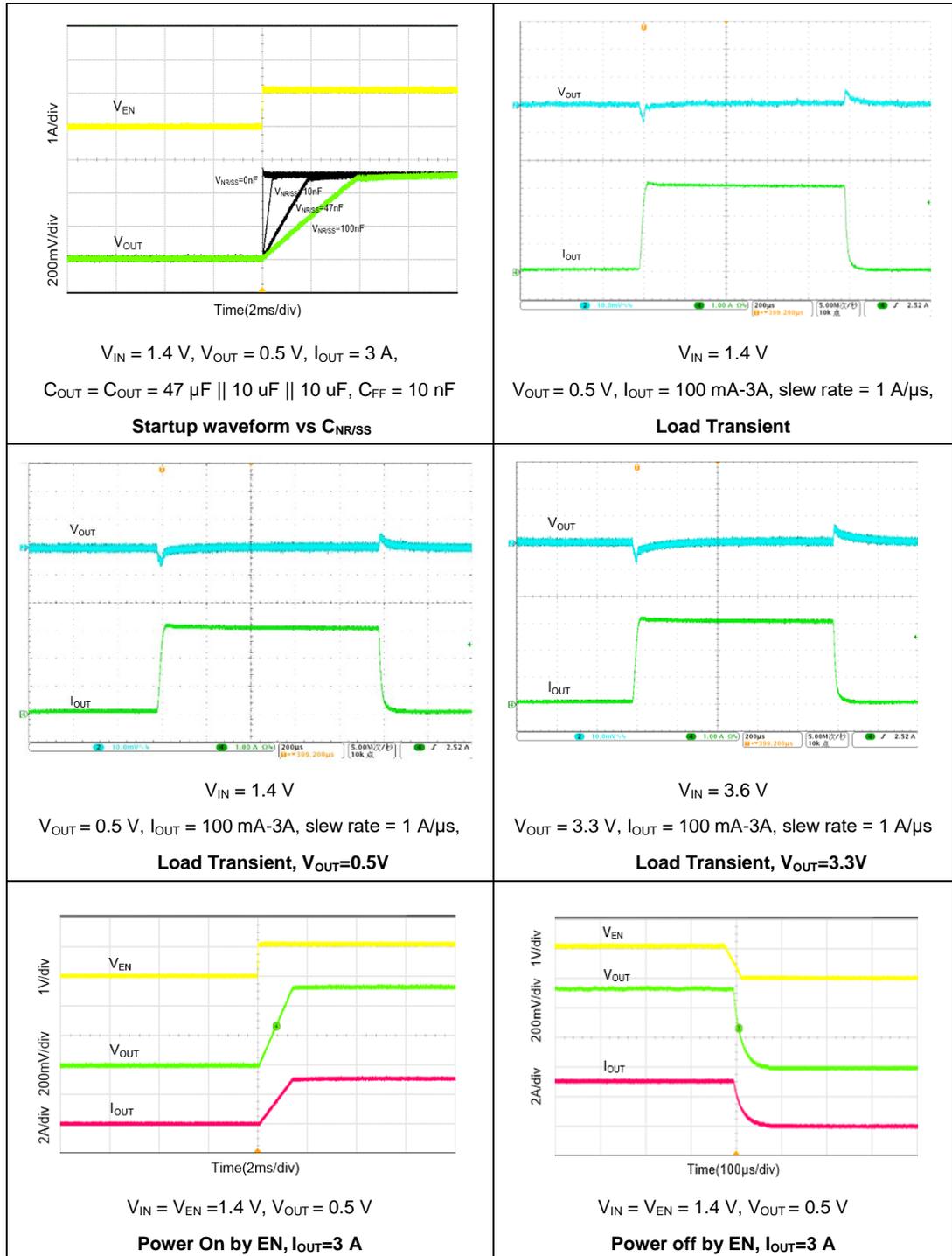
## Typical Characteristics

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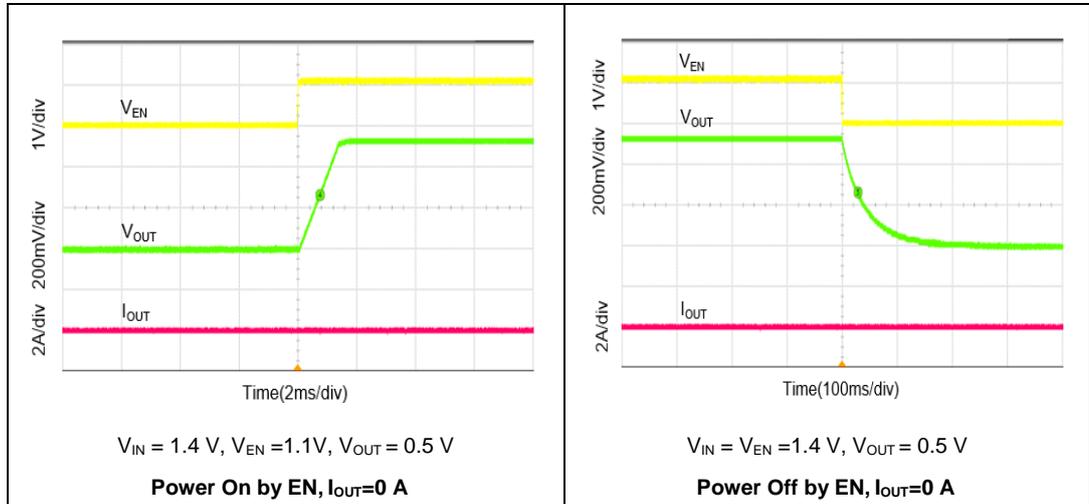
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## Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 1.4\text{ V}$  or  $V_{IN} = V_{OUT(NOM)} + 0.4\text{ V}$  (whichever is greater),  $V_{OUT(NOM)} = 0.5\text{ V}$ ,  $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 47\text{ }\mu\text{F} // 10\text{ }\mu\text{F} // 10\text{ }\mu\text{F}$  (unless otherwise noted).



## 7 Typical application circuit

Figure 7-1 Typical GD30LD1031x application circuit with adjustable resistance

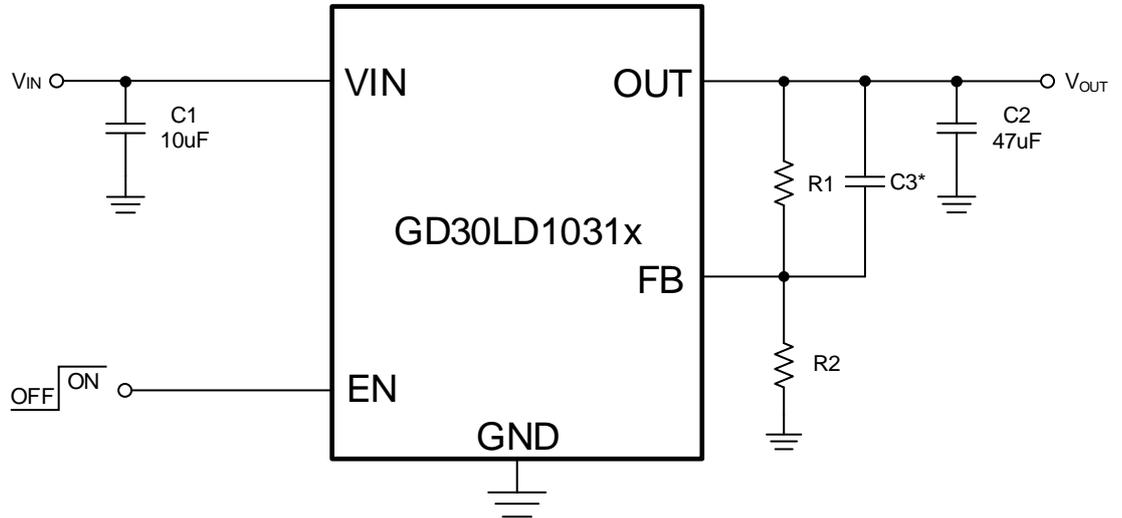
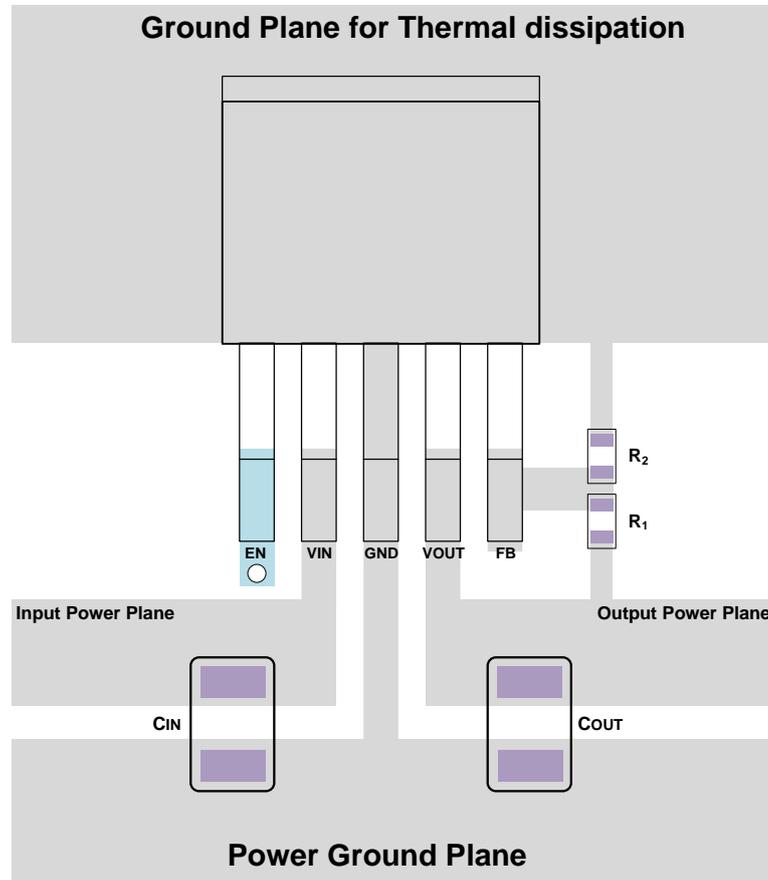


Table 7-1 Adjusted  $V_{OUT}$  by external feedback resistor

| $V_{OUT}(V)$ | External Feedback Resistor |                 |
|--------------|----------------------------|-----------------|
|              | R1 (k $\Omega$ )           | R2(k $\Omega$ ) |
| 0.5          | 0                          | NC              |
| 0.6          | 11                         | 54.9            |
| 0.7          | 10.2                       | 25.5            |
| 0.8          | 10.7                       | 17.8            |
| 0.9          | 11                         | 13.7            |
| 1.0          | 11                         | 11              |
| 1.2          | 9.31                       | 6.65            |
| 1.8          | 10.2                       | 3.92            |
| 2.5          | 10.8                       | 2.7             |
| 3.0          | 11                         | 2.2             |
| 3.3          | 11.2                       | 2               |
| 5.0          | 10.8                       | 1.2             |
| 5.2          | 12.22                      | 1.3             |

## 8 Layout guideline

Figure 8-1 Typical GD30LD1031x layout guideline



**Notes:**

1. The capacitor  $C_{IN}$  and  $C_{OUT}$  should be placed on the top layer to reduce parasitic parameters.
2. All capacitors are as close as possible to the corresponding pins of the LDO regulator.

## 9 Package information

### 9.1 TO263 package outline dimensions

Figure 9-1 TO263 package outline

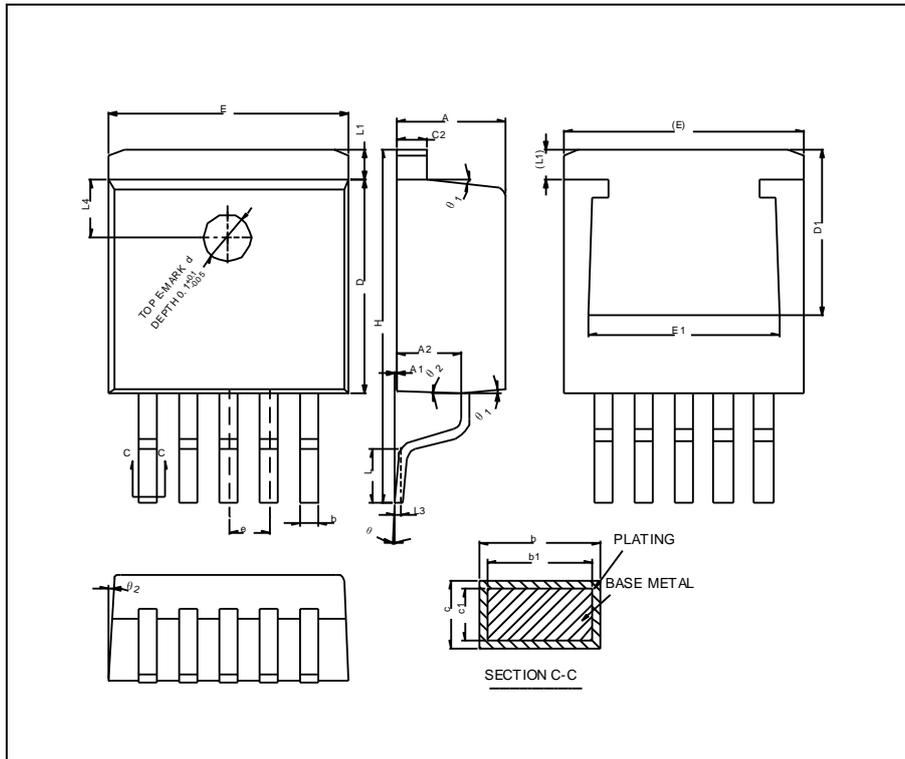


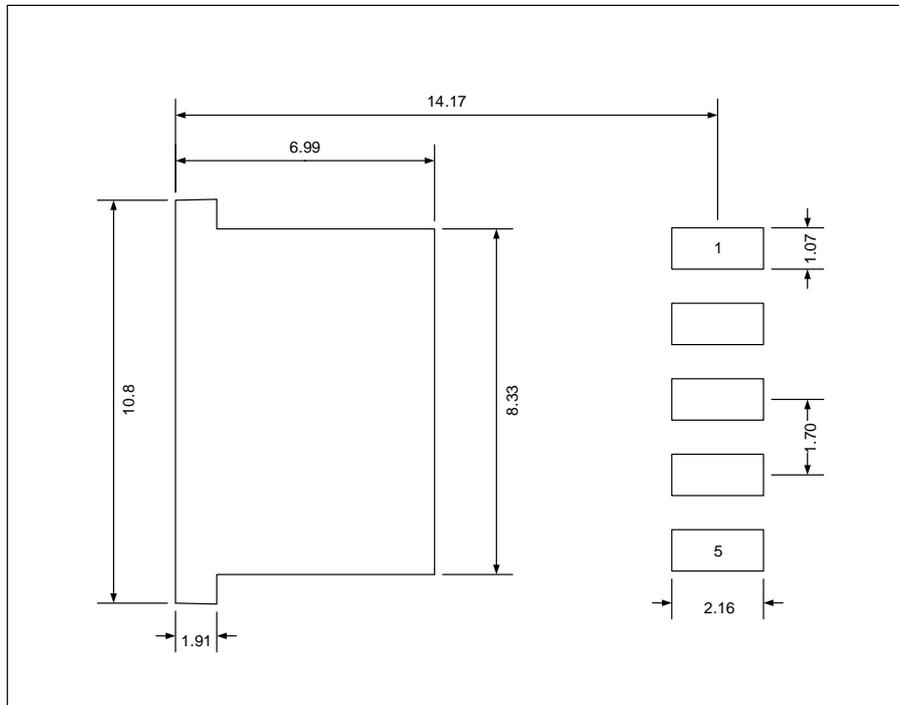
Table 9-1 TO263 package dimensions(in mm)

| Symbol | Min      | Nom   | Max   |
|--------|----------|-------|-------|
| A      | 4.40     | 4.57  | 4.70  |
| A1     | 0.00     | 0.10  | 0.25  |
| A2     | 2.59     | 2.69  | 2.79  |
| b      | 0.77     | —     | 0.90  |
| b1     | 0.76     | 0.81  | 0.86  |
| c      | 0.34     | —     | 0.47  |
| c1     | 0.33     | 0.38  | 0.43  |
| c2     | 1.22     | —     | 1.32  |
| d      | Ø2.0±0.1 |       |       |
| D      | 9.05     | 9.15  | 9.25  |
| D1     | 6.86     | —     | 7.50  |
| E      | 10.06    | 10.16 | 10.26 |
| E1     | 7.50     | —     | 8.30  |
| e      | 1.70BSC  |       |       |

| Symbol     | Min     | Nom   | Max   |
|------------|---------|-------|-------|
| H          | 14.70   | 15.10 | 15.50 |
| L          | 2.00    | 2.30  | 2.60  |
| L1         | 1.17    | 1.27  | 1.40  |
| L3         | 0.25BSC |       |       |
| L4         | 2.50REF |       |       |
| $\theta$   | 0°      | —     | 8°    |
| $\theta 1$ | 5°      | 7°    | 9°    |
| $\theta 2$ | 1°      | 3°    | 5°    |

(Original dimensions are in millimeters)

**Figure 9-2 TO263 recommend Footprint**



## 9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “ $\Theta$ ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\Theta_{JA}$ : Thermal resistance, junction-to-ambient.

$\Theta_{JB}$ : Thermal resistance, junction-to-board.

$\Theta_{JC}$ : Thermal resistance, junction-to-case.

$\Psi_{JB}$ : Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$ : Thermal characterization parameter, junction-to-top center.

$$\Theta_{JA} = (T_J - T_A)/P_D$$

$$\Theta_{JB} = (T_J - T_B)/P_D$$

$$\Theta_{JC} = (T_J - T_C)/P_D$$

Where,  $T_J$  = Junction temperature.

$T_A$  = Ambient temperature

$T_B$  = Board temperature

$T_C$  = Case temperature which is monitoring on package surface

$P_D$  = Total power dissipation

$\Theta_{JA}$  represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower  $\Theta_{JA}$  can be considerate as better overall thermal performance.  $\Theta_{JA}$  is generally used to estimate junction temperature.

$\Theta_{JB}$  is used to measure the heat flow resistance between the chip surface and the PCB board.

$\Theta_{JC}$  represents the thermal resistance between the chip surface and the package top case.

$\Theta_{JC}$  is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 9-2 TO263 Package thermal characteristics<sup>(1)</sup>**

| Symbol        | Condition                    | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| $\Theta_{JA}$ | Natural convection, 2S2P PCB | TO263   | 39.08 | °C/W |
| $\Theta_{JB}$ | Cold plate, 2S2P PCB         | TO263   | 19.15 | °C/W |
| $\Theta_{JC}$ | Cold plate, 2S2P PCB         | TO263   | 24.59 | °C/W |
| $\Psi_{JB}$   | Natural convection, 2S2P PCB | TO263   | 18.65 | °C/W |
| $\Psi_{JT}$   | Natural convection, 2S2P PCB | TO263   | 6.50  | °C/W |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

## 10 Ordering information

Table 10-1 Part ordering code for GD30LD1031x devices

| Ordering Code    | Package | Package Type | Packing Type | MOQ  | Temperature Junction Range |
|------------------|---------|--------------|--------------|------|----------------------------|
| GD30LD1031NBTR-I | TO263   | Green        | Tape&Reel    | 3000 | -40°C to +125°C            |

## 11 Revision history

Table 11-1 Revision history

| Revision No. | Description     | Date |
|--------------|-----------------|------|
| 1.0          | Initial Release | 2023 |

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